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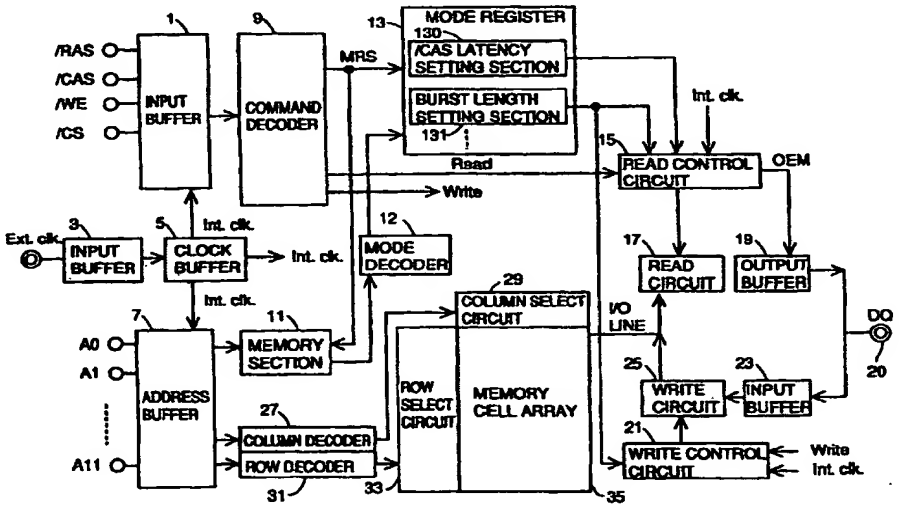
(54) SYNCHRONOUS TYPE SEMICONDUCTOR MEMORY DEVICE

(57) The present invention relates to a synchronous semiconductor memory device and an object of the present invention is to provide a synchronous semiconductor memory device in which an operation mode such as a set burst length would not be lost even at the power off. Here, the synchronous semiconductor memory device according to the present invention includes non-volatile memory means (11, 12, 13) for storing operation mode and controlling data reading operation and data writing operation in accordance therewith.

FIG. 1



EP 0 929 075 A1

Description

Field of the Art

[0001] The present invention relates generally to a semiconductor memory device, and more particularly to a synchronous semiconductor memory device operating in synchronization with a clock signal.

Background of the Art

[0002] In a synchronous semiconductor memory device (hereinafter referred to as an SDRAM) now available as a commercial product, Burst Length (BL), /CAS Latency (CL) and so on can be set in a mode register included in the device by a user at its use.

[0003] Here, Burst Length is a number of data read out or written into in sequence in one access cycle. In an SDRAM, BLs of 1, 2, 4 or 8 are available and some chips have a full page mode. /CAS Latency is a number of clock cycles elapsed from application of read instruction until an output of data from an output buffer. In an SDRAM, CLs=2, 3 in general are available and in some chips, CL=1, 4.

[0004] Though operation modes such as Burst Length and /CAS latency set in the mode register do not change until reset, at the power off the mode register is reset and the set information is lost.

Disclosure of the Invention

[0005] An object of the present invention is to provide a synchronous semiconductor memory device wherein a set operation mode is not lost even at the power off.

[0006] The object of the present invention is achieved by providing a synchronous semiconductor memory device including a memory storing data, a clock buffer generating an internal dock signal by buffering an external clock signal, an input buffer generating an internal control signal in response to the internal dock signal by buffering an external control signal, an address buffer generating an internal address signal in response to the internal clock signal by buffering an external address signal, a read circuit reading data from the memory, a write circuit writing external data into the memory, and, a non-volatile memory section storing an operation mode in accordance with the internal control signal and the internal address signal and controlling the read circuit and the write circuit in accordance with the operation mode.

[0007] A main advantage of the present invention lies in that the synchronous semiconductor memory device can be restarted in an operation mode stored in the non-volatile memory section without need of operation mode setting at the next power on after the power off, because the operation mode is stored in the non-volatile memory section.

Brief Description of the Drawings

[0008]

Fig. 1 is a block diagram of a synchronous semiconductor memory device in accordance with a best mode for carrying out the present invention, and
Fig. 2 is a schematic block diagram of a memory section and a mode decoder shown in Fig. 1, referenced for describing their operations.

The Best Mode for Carrying Out the Invention

[0009] Hereinafter with reference to the drawings, a synchronous semiconductor memory device as a best mode for carrying out the present invention will be described In the drawings, the same character indicates the same or corresponding element.

[0010] With reference to Fig. 1, the synchronous semiconductor memory device in accordance with the present invention includes a data input/output terminal 20, a memory cell array 35 storing external data supplied as an input to data input/output terminal 20, a row select circuit selecting a row in memory cell array 35 to which data is to be written into or from which data is to be read out, a column select circuit 29 selecting a column to which data is to be written into or from which data is to be read out, an input buffer 3 buffering an external clock signal Ext. clk., a clock buffer 5 generating a internal dock signal Int. clk. by buffering an output signal from input buffer 3, an input buffer 1 generating an internal control signals by receiving and buffering external control signals such as a row address strobe signal /RAS, a column address strobe signal /CAS, a write enable signal /WE, or a chip select signal /CS in synchronization with internal clock signal Int.clk. generated by clock buffer 5, an address buffer 7 generating an internal address signal by receiving and buffering external address signal (A0-A11) in synchronization with the internal clock signal Int. clk., a column decoder 27 driving column select circuit 29 by decoding a column address signal in the internal address signal, a row decoder 31 driving row select circuit 33 by decoding a row address signal in the internal address signal, a command decoder 9 generating and supplying as an output a read instruction signal Read, a write instruction signal Write, and a mode register set signal MRS in accordance with a combination of row address strobe signal /RAS, column address strobe signal /CAS and write enable signal /WE sent to input buffer 1 as inputs, a mode register 13 including a /CAS Latency setting section 130, a Burst Length setting section 131, a burst type setting section (not shown) and so on, and setting an operation mode such as /CAS Latency or Burst Length in accordance with a combination of external address signal bits A0-A11 supplied as an input to address buffer 7 in response to an input of mode register set signal MRS, a memory section 11 storing the

internal address signal and mode register set signal MRS for setting the operation mode, a mode decoder 12 decoding and supplying a signal stored in memory section 11 to mode register 13, a read control circuit 15 generating an output enable signal OEM and a read control signal in accordance with the operation mode set in mode register 13 and in response to internal clock signal Int. clk. and read instruction signal Read, a read circuit 17 reading out data stored in memory cell array 35 in response to the read control signal, an output buffer 19 being activated by output enable signal OEM and buffering and supplying as an output data read out by read circuit 17 to data input/output terminal 20, a write control circuit 21 generating a write control signal in accordance with the operation mode set in mode register 13, and in response to internal clock signal Int. clk. and write instruction signal Write, an input buffer 23 buffering external data supplied as an input to data input/output terminal 20 and a write circuit 25 writing into memory cell array 35 data supplied as an output from input buffer 23 in response to the write control signal.

[0011] Fig. 2 is a schematic diagram showing configurations of memory section 11 and mode decoder 12.

[0012] As shown in Fig. 2, memory section 11 includes, for example, two non-volatile memory elements 110 and 111 each storing 1 bit information, and mode decoder 12 includes an inverter, and an NAND circuit.

[0013] Next, the operation of the synchronous semiconductor memory device will be described.

[0014] When row address strobe signal /RAS, column address strobe signal /CAS, write enable signal /WE and chip select signal /CS are all supplied as an input to input buffer 1 in a logical low level state in response to the internal clock signal, command decoder 9 supplies, as an output, mode register set signal MRS to mode register 13.

[0015] The mode register set signal MRS is stored in memory section 11 until a next mode register set signal MRS is supplied as an output from command decoder 9.

[0016] Mode register 13 having received the mode register set signal MRS, stores in memory section 11 a combination of external address signal bits A0-A11 supplied as an input to address buffer 7 and sets /CAS Latency and Burst Length respectively in /CAS Latency setting section 130 and Burst Length setting section 131 according to the combination. In particular, Burst Length is designated by combination of external address signal bits A0, A1 and A2 and /CAS Latency is designated by combination of external address signal bits A4, A5 and A6.

[0017] Here, on receiving read instruction signal Read, read control circuit 15 controls read circuit 17 in accordance with /CAS Latency and Burst Length set in mode register 13 in synchronization with internal clock signal Int. clk. and supplies as an output, output enable signal OEM for activating output buffer 19.

[0018] On the other hand, on receiving write instruction signal Write, write control circuit 21 controls write circuit 25 in accordance with Burst Length set in mode register 13 in synchronization with internal clock signal Int. clk.

[0019] When the synchronous semiconductor memory device is powered off, /CAS Latency and Burst Length set in mode register 13 are lost. At the power on, however, /CAS Latency, Burst Length and so on are set again in mode register 13 to the same values as immediately before the power off in accordance with the mode register set signal MRS and the internal address signal stored in memory section 11.

[0020] Operations of memory section 11 and others will be described referring to Fig. 2.

[0021] Assume that memory section 11 includes two 1-bit non-volatile memory elements 110 and 111, for example, that store address information (X,Y). If (0, 0) is stored as (X,Y) at the power off, memory section 11 supplies (0, 0) as an output at the power on, and an output signal A from an inverter 120 of mode decoder 12 will be "1" and output signals B, C, and D from inverters 121, 122, and 123 will be all "0". Thus the operation modes such as /CAS Latency, which is determined by the signal A taking the value "1", are reset.

[0022] When (0, 1) is stored as (X, Y), only the output signal B from inverter 121 is "1". If (1, 0) is stored, only the signal C, and if (1, 1) is stored, only the signal D is "1".

[0023] Particularly, an EPROM (Electrically Programmable Read Only Memory), an EEPROM (Electrically Erasable and Programmable Read Only Memory) or the like can be used as the non-volatile memory elements 110 and 111. If the element is overridable, rewriting is possible for a number of times.

[0024] With the synchronous semiconductor memory device described above, troublesome setting of operation modes such as /CAS Latency at the power on can be avoided, because information for setting operation modes such as /CAS Latency and Burst Length is stored in memory section 11 including the non-volatile memory element.

[0025] In the foregoing, memory section 11 may be included in mode register 13 and stores mode register set signal MRS supplied as an input to mode register 13 and an output signal from mode decoder 12. The same advantages can be obtained as well when memory section 11 is in mode register 13 and stores an output signals from /CAS Latency setting section 130 and Burst Length setting section 131.

Claims

1. A synchronous semiconductor memory device, comprising:

   a memory (35) storing data;

clock signal buffering means (3, 5) for buffering an external clock signal to generate an internal clock signal;

input buffering means (1) responsive to the internal dock signal for buffering an external clock signal to generate an internal control signal;

address buffering means (7) responsive to the internal clock signal for buffering an external address signal to generate an internal address signal;

data reading means (15, 17) for reading out said data from said memory;

data writing means (21, 25) for writing external data into said memory; and

non-volatile memory means (11, 12, and 13) for storing an operation mode in response to said internal control signal and said internal address signal and controlling said data reading means and said data writing means in accordance with said operation mode.

2. A synchronous semiconductor memory device, comprising:

a memory (35) storing data;

clock signal buffering means (3, 5) for buffering an external clock signal to generate an internal clock signal;

input buffering means (1) responsive to said internal clock signal for buffering an external control signal to generate an internal control signal;

address buffering means (7) responsive to said internal clock signal for buffering an external address signal to generate an internal address signal;

mode setting means (13) in which operation mode can be set designating a reading procedure of said data from said memory and a writing procedure of external data into said memory;

data reading means (15, 17) for reading said data stored in said memory in response to said operation mode set in said mode setting means and in response to said internal clock signal and a read signal;

data writing means (21, 25) for writing external data into said memory in response to said operation mode set in said mode setting means and in response to said internal clock signal and a write signal;

instruction means (9) for generating a mode set signal for setting said operation mode in said mode setting means in response to said internal control signal ad generating said read signal and said write signal; and

non-volatile memory means (11) for storing said mode set signal and said internal address signal and supplying said stored mode set signal and said stored internal address signal to said mode setting means.

FIG. 1

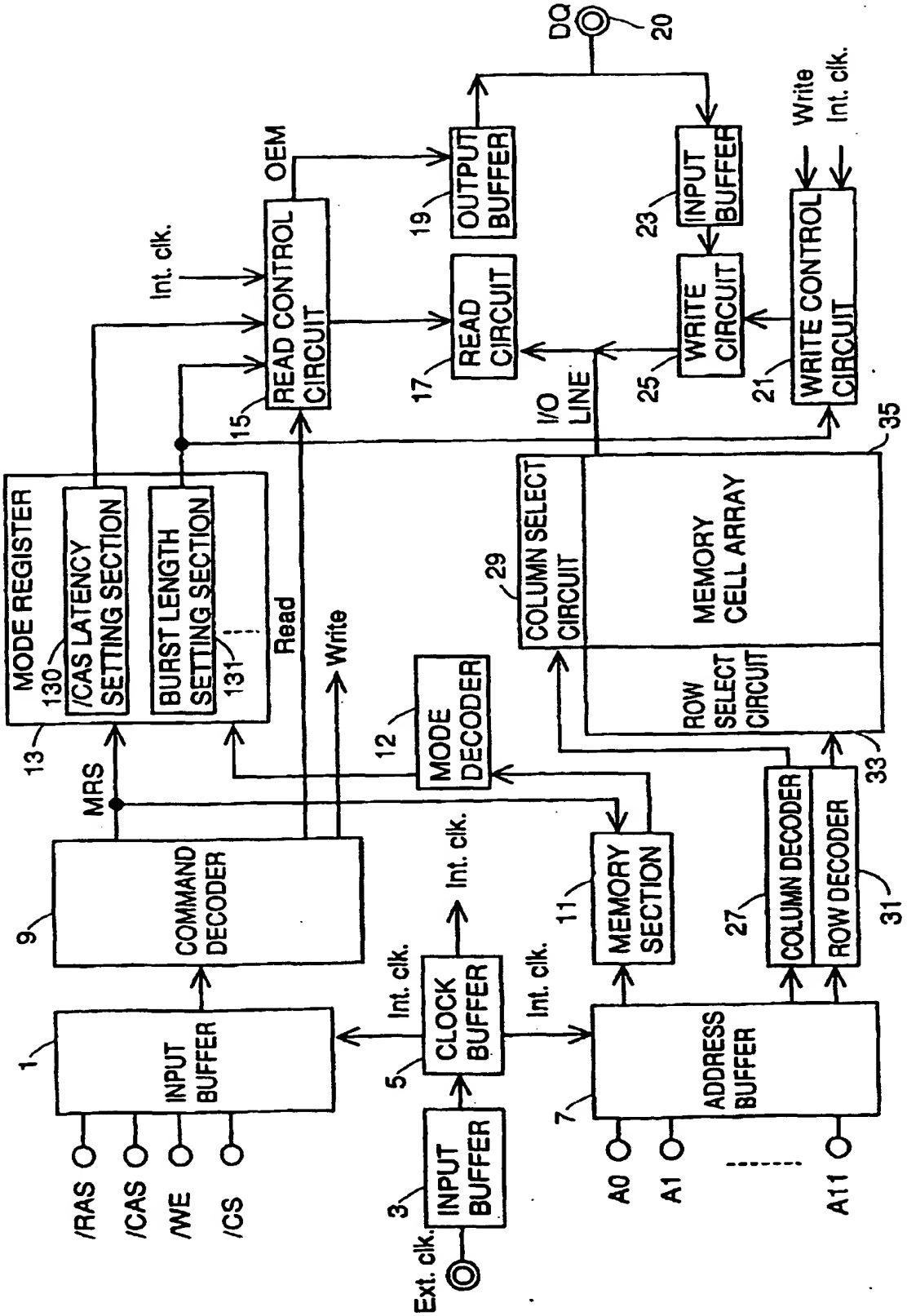
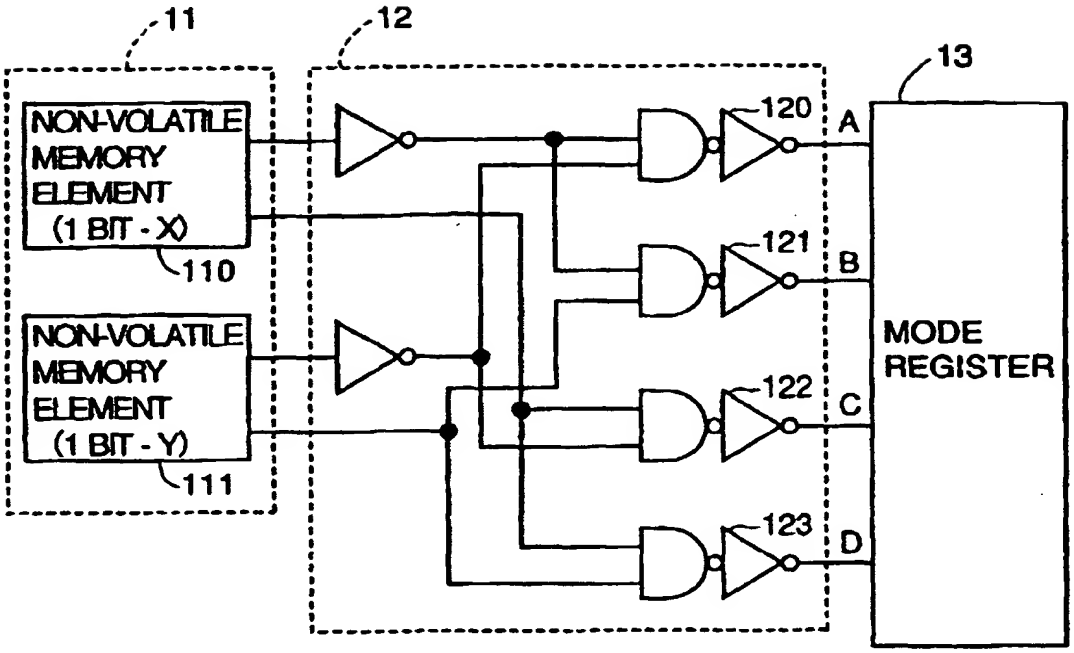

/RAS
/CAS
/WE
/CS
Ext. clk.
A0
A1
A11
DQ
20
INPUT BUFFER
1
3
CLOCK BUFFER
5
ADDRESS BUFFER
7
COMMAND DECODER
9
MEMORY SECTION
11
MODE DECODER
12
MODE REGISTER
13
130
/CAS LATENCY SETTING SECTION
131
BURST LENGTH SETTING SECTION
READ CONTROL CIRCUIT
15
OEM
READ CIRCUIT
17
OUTPUT BUFFER
19
WRITE CIRCUIT
25
INPUT BUFFER
23
WRITE CONTROL CIRCUIT
21
COLUMN DECODER
27
ROW DECODER
31
ROW SELECT CIRCUIT
33
COLUMN SELECT CIRCUIT
29
MEMORY CELL ARRAY
35
I/O LINE
MRS
Int. clk.
Read
Write
Write Int. clk.

FIG. 2


11
12
13
NON-VOLATILE MEMORY ELEMENT (1 BIT - X)
110
NON-VOLATILE MEMORY ELEMENT (1 BIT - Y)
111
120
121
122
123
A
B
C
D
MODE REGISTER

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP96/02781

A. CLASSIFICATION OF SUBJECT MATTER
Int. Cl^6 G11C11/407

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int. Cl^6 G11C11/407, G06F15/78

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1926 - 1996
Kokai Jitsuyo Shinan Koho 1971 - 1996

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP, 63-206852, A (Hitachi Maxell, Ltd.), August 26, 1988 (26. 08. 88)(Family: none)	1, 2
A	JP, 07-93970, A (Fujitsu Ltd.), April 7, 1995 (07. 04. 95)(Family: none)	1, 2
A	JP, 08-124380, A (Hitachi, Ltd.), May 17, 1996 (17. 05. 96)(Family: none)	1, 2

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
December 17, 1996 (17. 12. 96)	January 8, 1997 (08. 01. 97)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)